

A circular black ink stamp from the Intellectual Property Office (IPO). The text "O I P E" is curved along the top inner edge, and "J C E O" is curved along the top outer edge. The date "AUG 10 2005" is stamped in the center. The words "PATENT & TRADEMARK OFFICE" are curved along the bottom inner edge.

The diagram illustrates a system for converting serial data to parallel data while synchronizing the output clock with the input clock. The system consists of the following components and signal paths:

- Input Stage:** **INPUT DATA** (d1) enters a **SERIAL / PARALLEL CONVERTER** (101). **INPUT CLOCK** (c11) enters a **FREQUENCY DIVIDER** (105).
- Control and Addressing:** The output of 101 passes through a **DESTUFFING CONTROL CIRCUIT** (104) to a **BUFFER MEMORY** (102). The output of 105 (c12) also feeds into 102. A **WRITE ADDRESS COUNTER** (106) receives c12 and provides an address to 102. A **READ ADDRESS COUNTER** (113) receives a clock signal (c14) and provides an address to 102.
- PLL Core (120):** A dashed box containing:
 - FREQUENCY DIVIDER** (107) receiving c12.
 - FREQUENCY DIVIDER** (111) receiving c14.
 - PHASE COMPARATOR** (108) receiving inputs from 107 and 111.
 - LPF** (109) receiving the output of 108.
 - VCO** (110) receiving the output of 109.
- Output Stage:** The output of 102 goes to a **PARALLEL / SERIAL CONVERTER** (103). The output of 110 (c15) passes through an **LPF** (109) and a **FREQUENCY DIVIDER** (112) to produce the **OUTPUT CLOCK**.

(Prior ART)

REPLACEMENT FIGURE

FIG. 8 A (PRIOR ART)

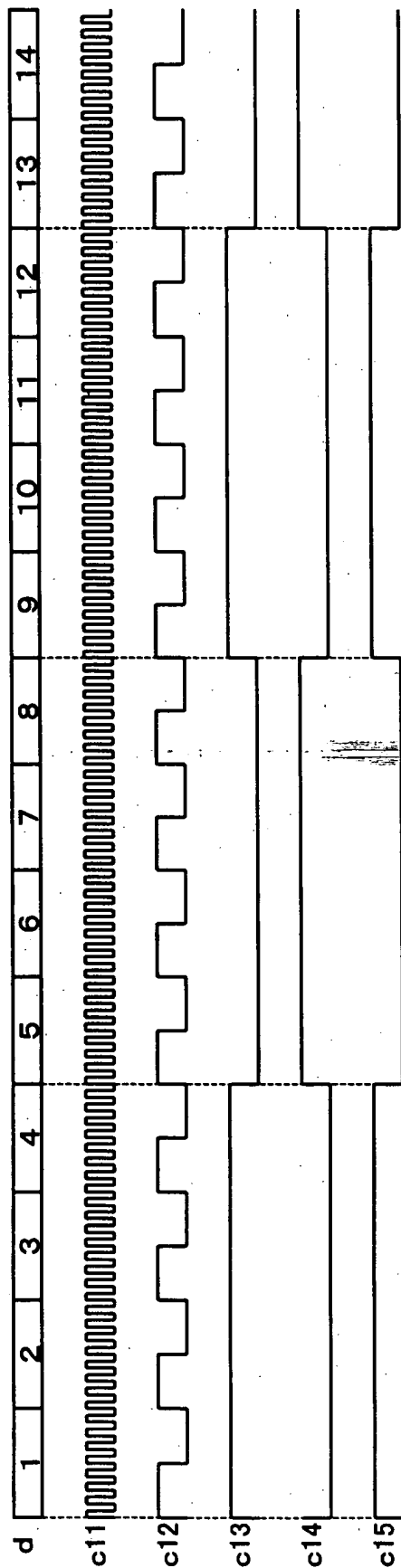
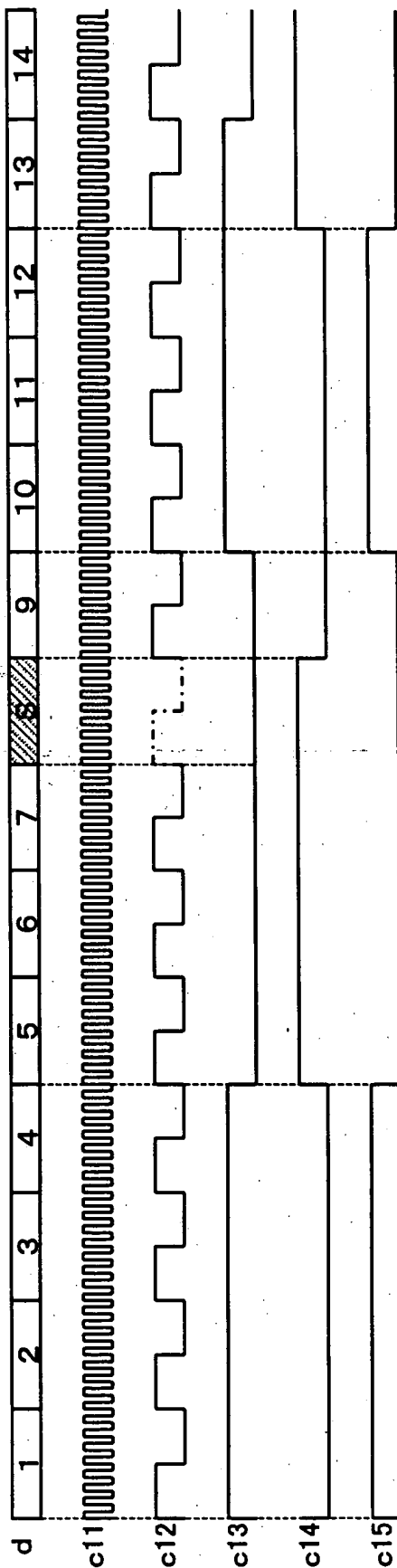
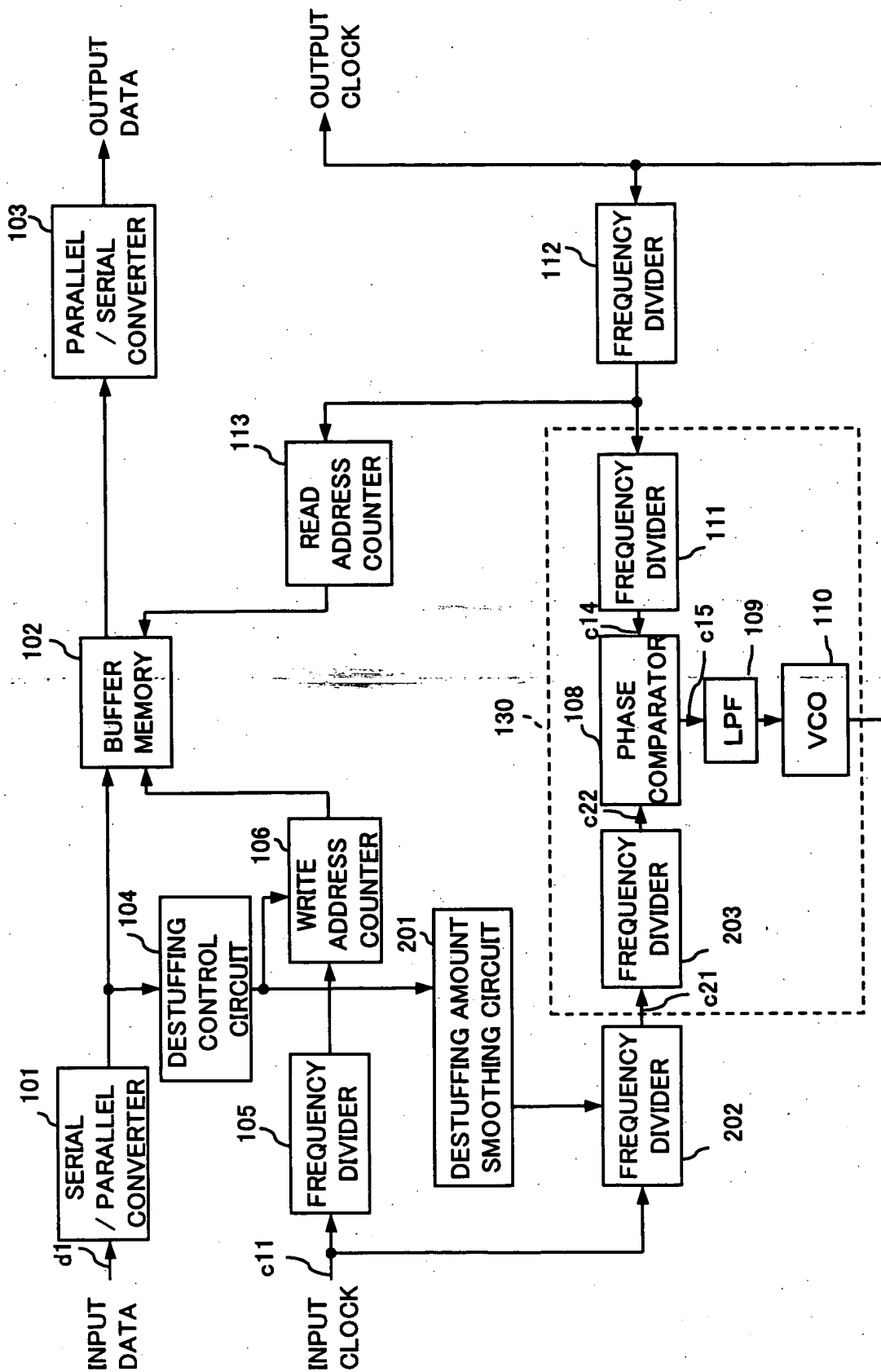


FIG. 8 B (PRIOR ART)



REPLACEMENT FIGURE
 FIG. 9 (Prior Art)



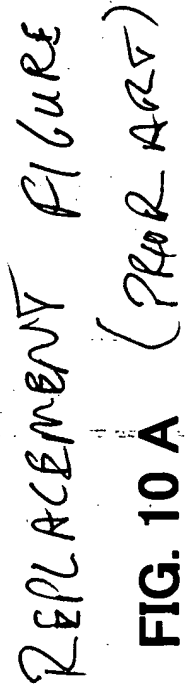


FIG. 10 A

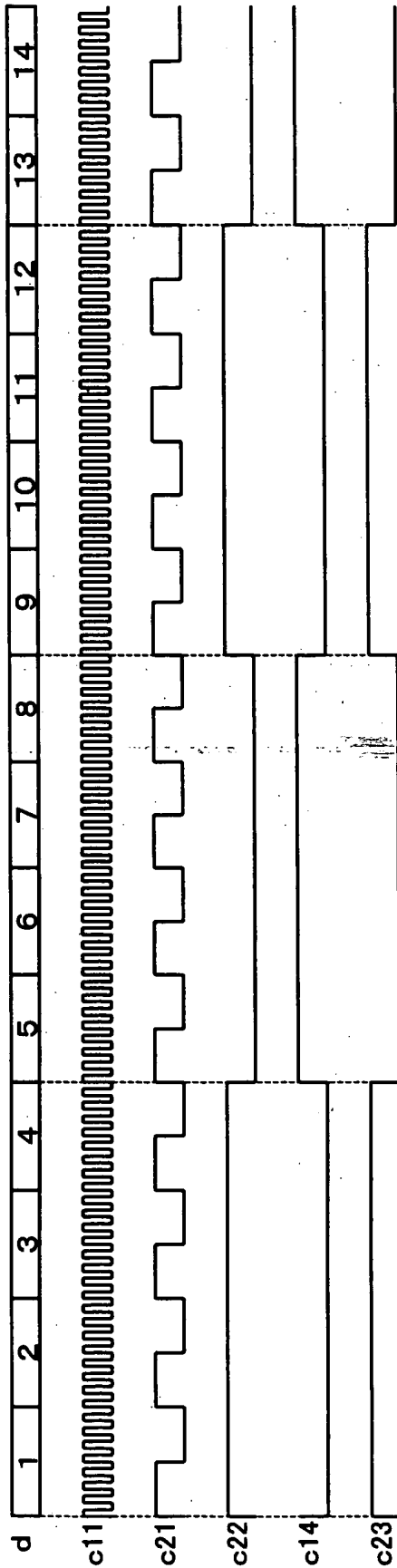


FIG. 10 B

